ABSTRACT

CIRCUIT FOR ACCESSING A CHALCOGENIDE MEMORY ARRAY

A circuit for accessing a chalcogenide memory array is disclosed. The chalcogenide memory array includes multiple subarrays with rows and columns formed by chalcogenide storage elements. The chalcogenide memory array is accessed by discrete read and write circuits. Associated with a respective one of the subarrays, each of the write circuits includes an independent write 0 circuit and an independent write 1 circuit. Also associated with a respective one of the subarrays, each of the read circuits includes a sense amplifier circuit. In addition, a voltage level control module is coupled to the read and write circuits to ensure that voltages across the chalcogenide storage elements within the chalcogenide memory array do not exceed a predetermined value during read and write operations.